

Produced By:

**Commodore International Spare Parts GmbH
Braunschweig, West Germany**

Service Manual

CD32 / SPELLBOUND

CD/GS PLAYER

05 / 27 / 1993

INTERNATIONAL EDITION

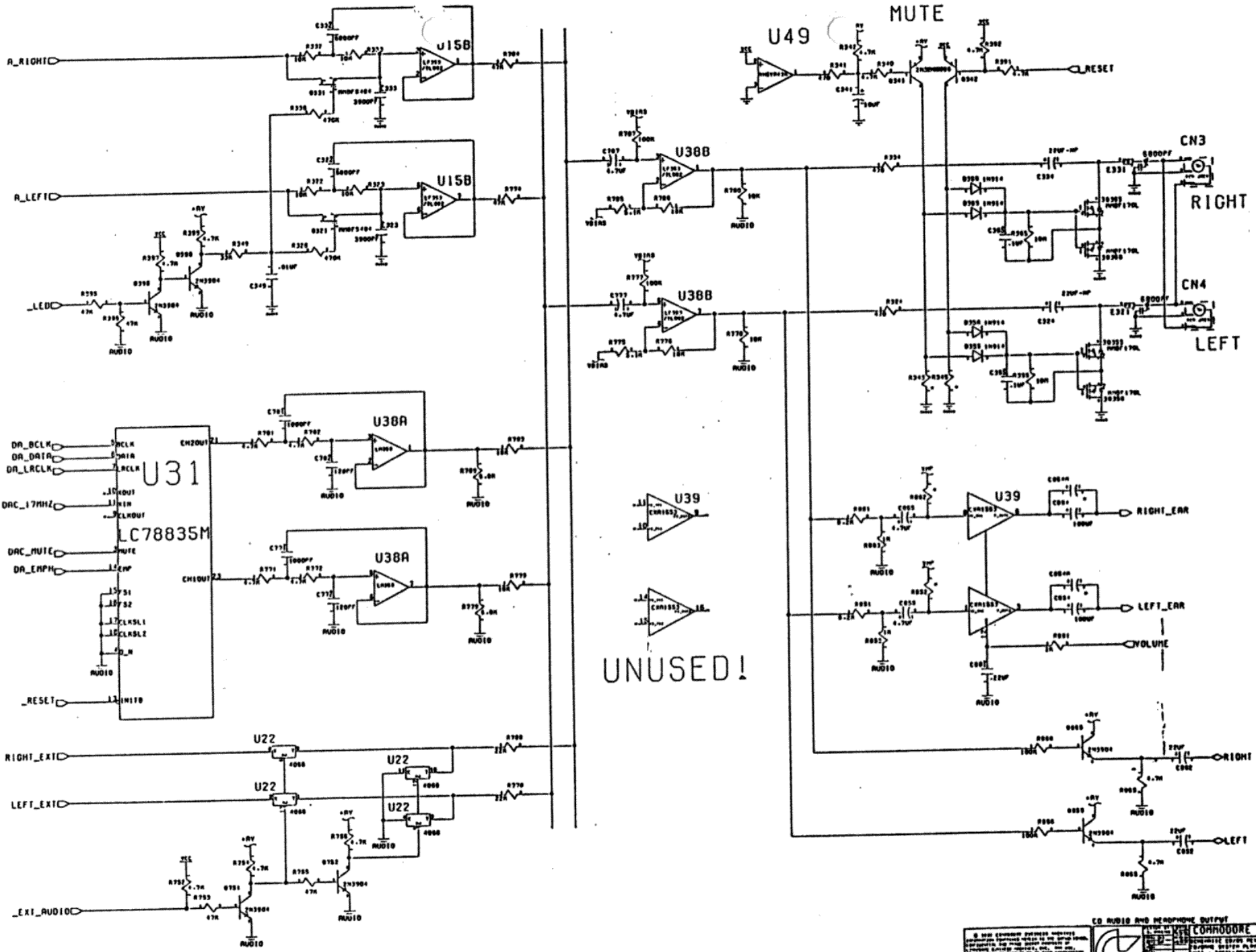
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CD/GS PLAYER PCB

CD AUDIO AND HEADPHONE OUTPUT

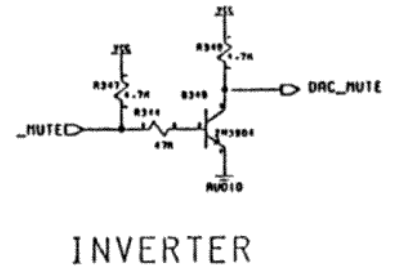
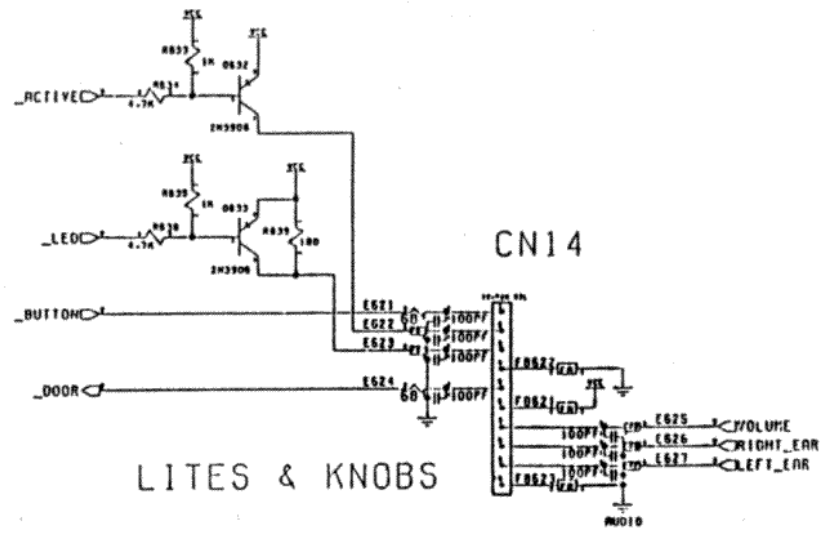
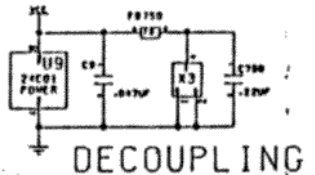
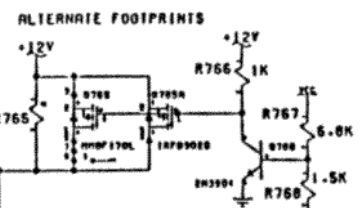
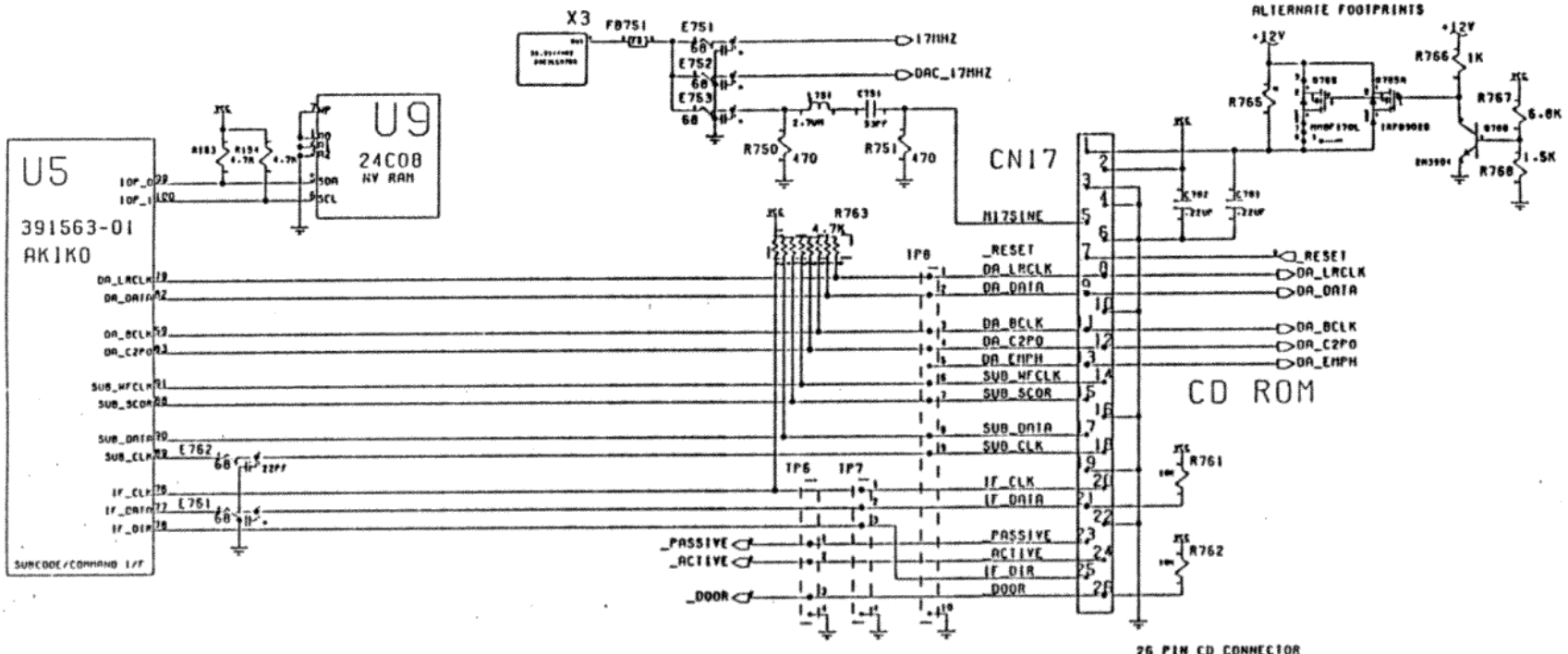
CONTOUR

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DATE 8/11

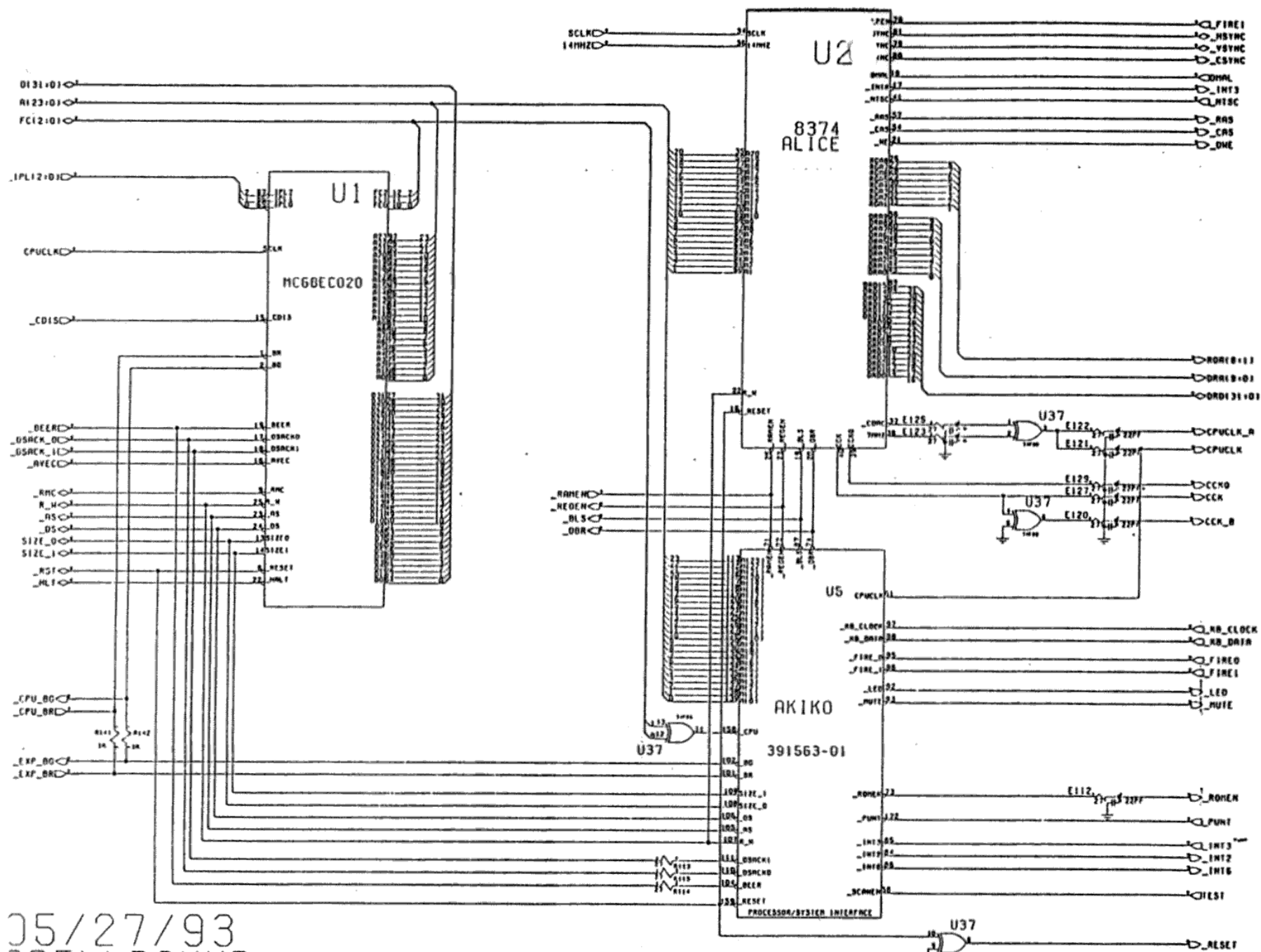
100% QUALITY CONTROL

CD/GS PLAYER PCB



CD ROM, THE WAVE OF THE FUTURE - MGT

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 SPELLBOUND
 CD/GS PLAYER PCB

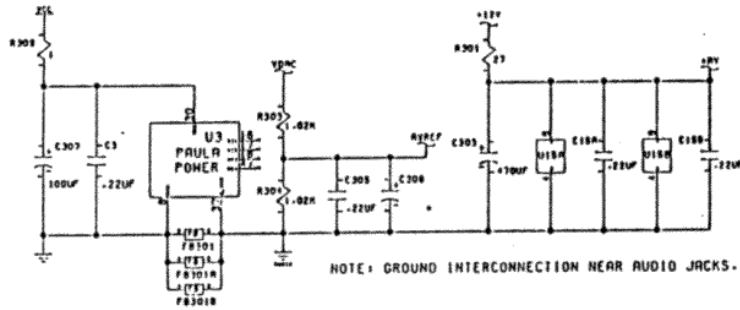
NOTE: VARIOUS COMPONENTS ARE FOR ENI CONTROL
 AND MAY BE LOADED WITH FUNNY THINGS...

PROCESSOR AND OTHER USEFUL COMPONENTS

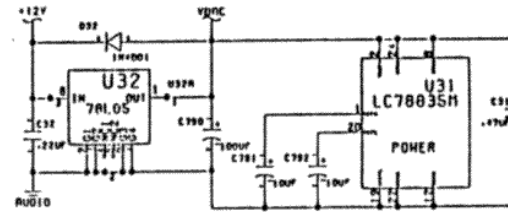
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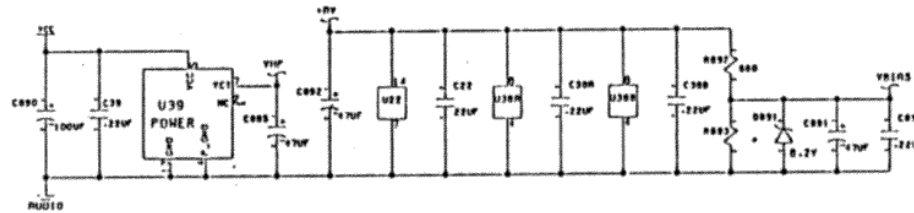
PAULA/AUDIO DECOUPLING



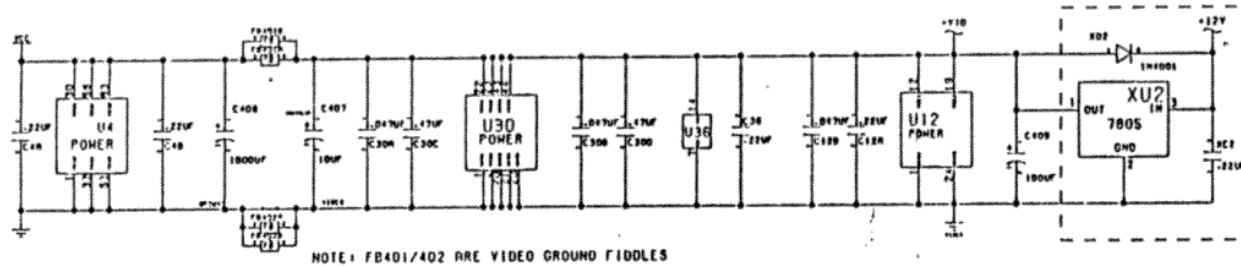
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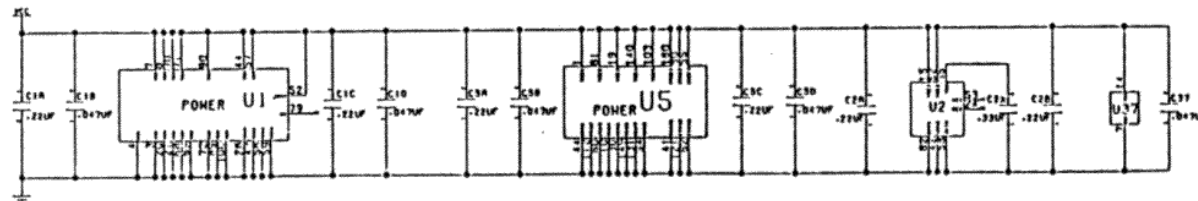
HEADPHONE/AUDIO DECOUPLING



VIDEO DECOUPLING



PROCESSOR/GATOR/ALICE DECOUPLING



CD/GS PLAYER PCB

POWER MANAGEMENT & DECOUPLING DESIGN

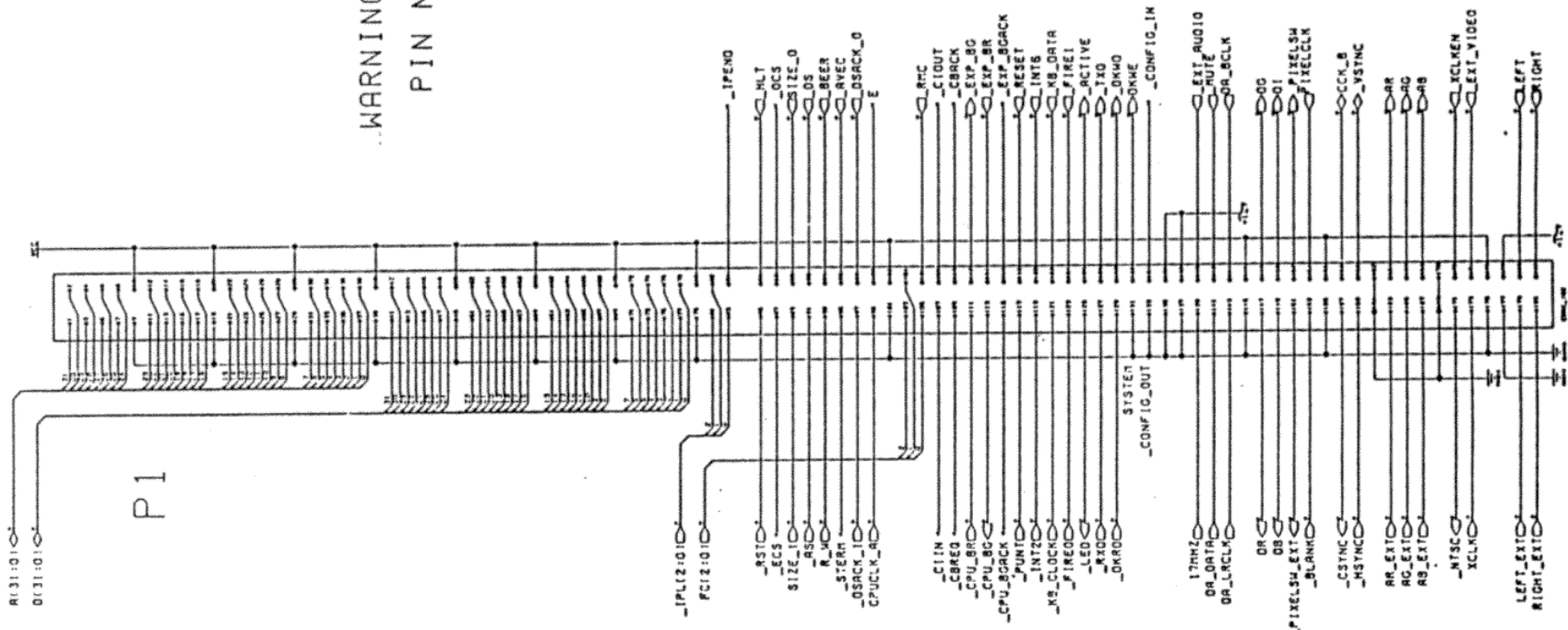
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DATE: 01/18/98
 DRAWN BY: J. S. GEMERTIS
 CHECKED BY: J. S. GEMERTIS
 APPROVED BY: J. S. GEMERTIS

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EXPANSION CONNECTOR



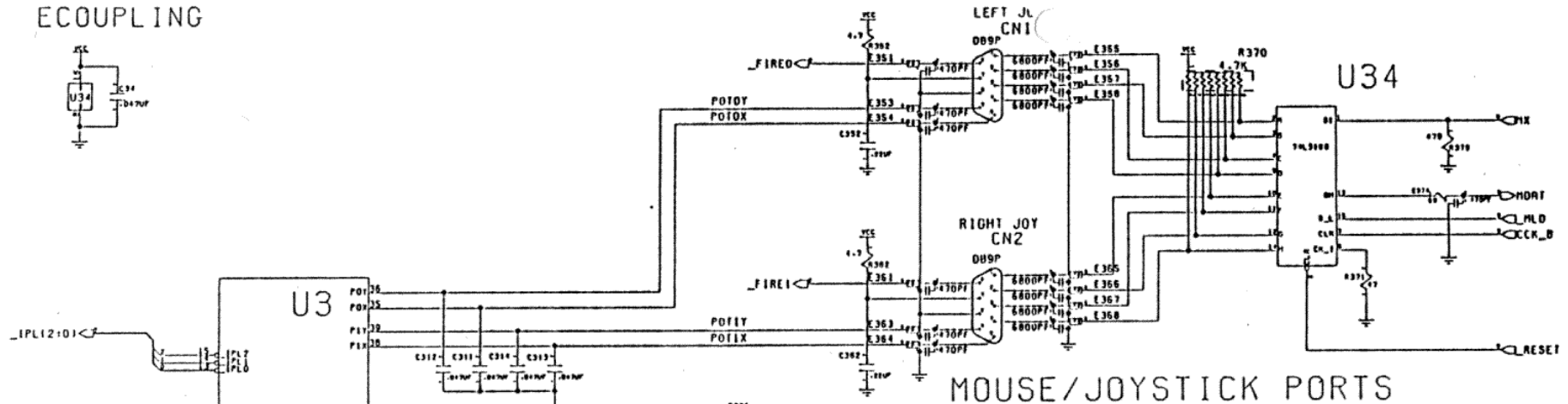
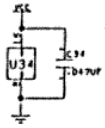
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WARNING:
PIN NUMBERS ARE BACKWARDS

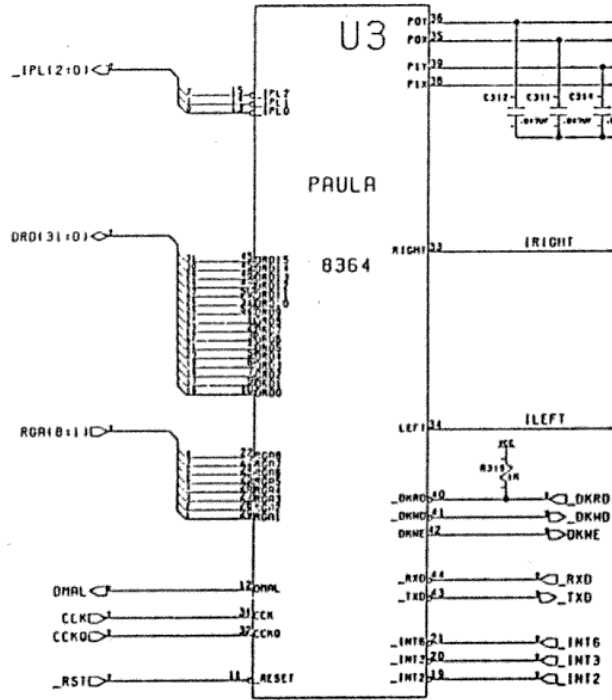
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CD/GS PLAYER PCB

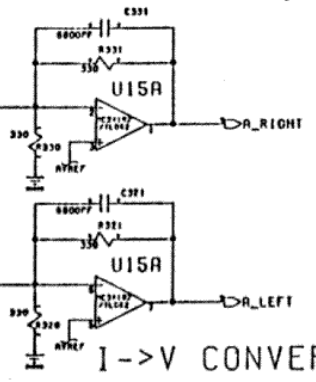
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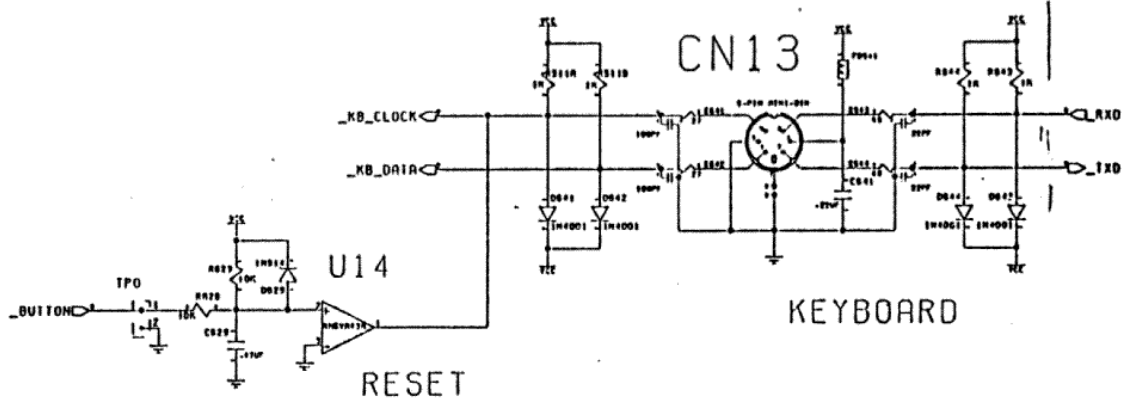
MOUSE/JOYSTICK PORTS



PAULA
8364



I->V CONVERTER



KEYBOARD

RESET

CD/GS PLAYER PCB

PAULA PREFERS THE TRADITIONAL MODES

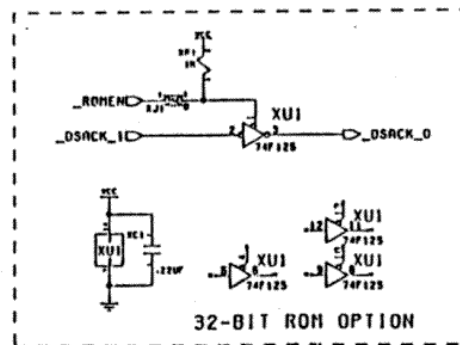
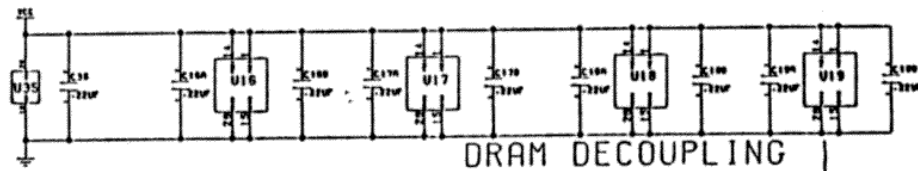
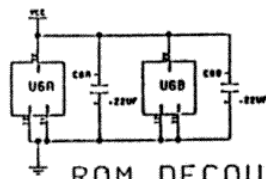
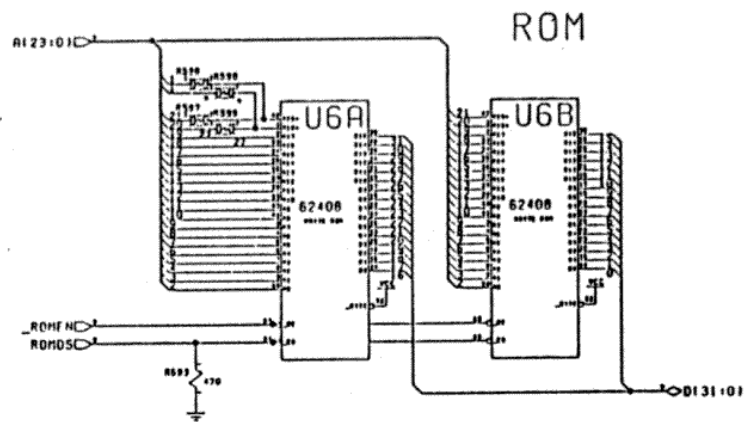
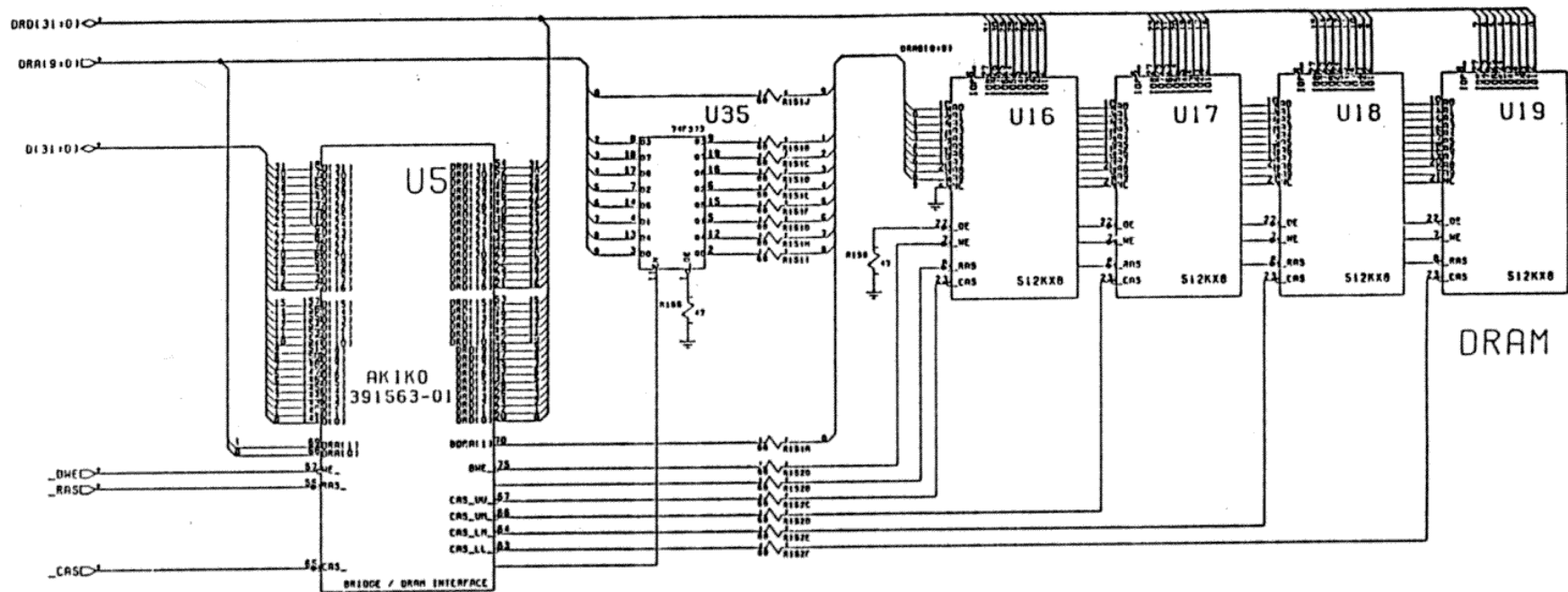
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KEYBOARD

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DATE: 11/88

REV: 1.0



CD/GS PLAYER PCB

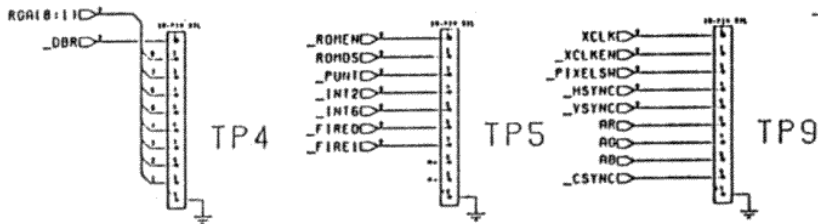
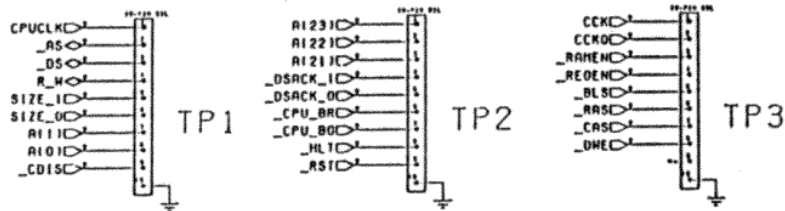
ROM DECOUPLING

REPORT AND... WILL BE USED TO REGENERATE

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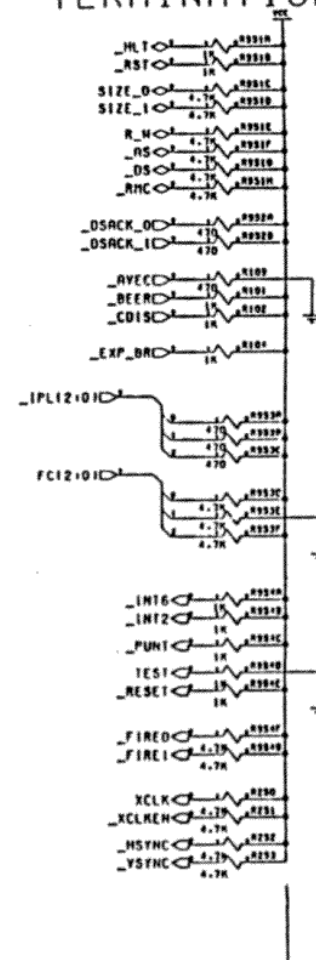
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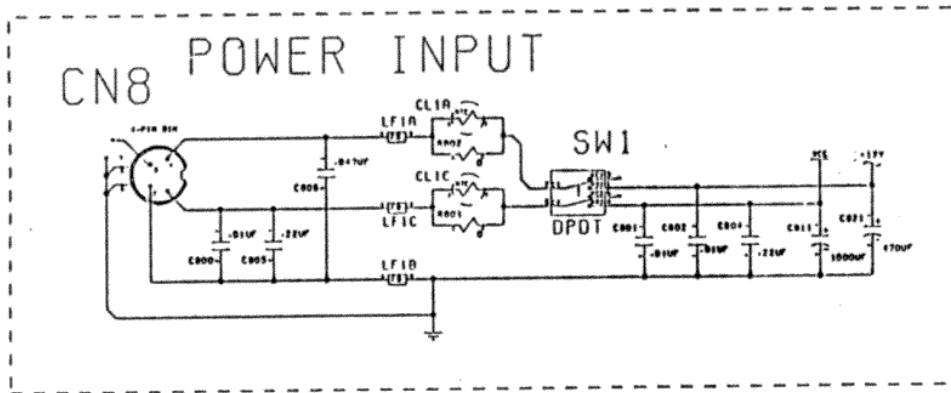
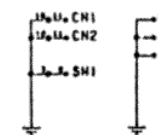


TEST ACCESS

TERMINATION



HOLES & C.



CD/GS PLAYER PCB

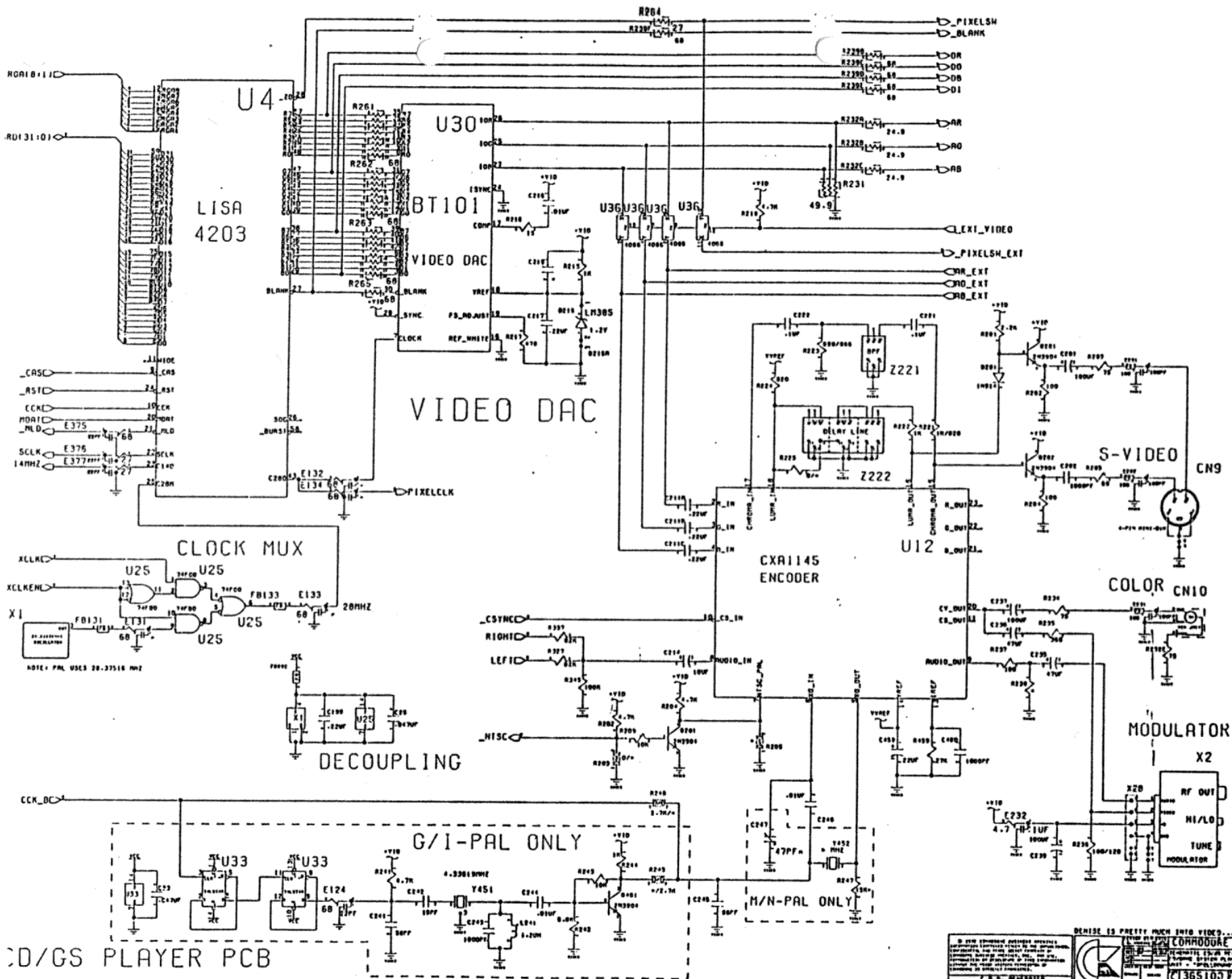
USER INTERFACE AND RELATED HARDWARE

COMMODORE

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REV	DESCRIPTION	DATE	BY
0	ENGINEERING PROTOTYPE	10/24/83	CHR
0A	DEVELOPER/PROF'S RELEASE	5/18/84	CHR
1	ADVANCE ENGINEERING RELEASE	5/18/84	CHR
2	Revised per ECO 830008	7/1/83	
A	PILOT PRODUCTION RELEASE	10/83	
A	Revised per ECO 830162	10-13-83	B.M.
C	REVISED PER ECO 910117 (M)	7/7/84	
D	REVISED PER ECO 920212	6-13-84	B.M.
E	REVISED...		

WC3267

7/15/93

SIGNAL GLOSSARY

SIGNAL	DESCRIPTION (AREA)	PAGES
Z8MHz	28.63636 MHz MASTER CLOCK	
ZMHz	7.15909 MHz PROCESSOR CLOCK	
A(23:1)	PROCESSOR ADDRESS BUS (60000)	
DATA	DATA MEMORY (PARALLEL PORT)	
AS	ADDRESS STROBE (60000)	
AUDIOIN	AUDIO INPUT (AS232 JACK)	
AUDIOOUT	AUDIO OUTPUT (AS232 JACK)	
CELR	BUS ERROR (60000)	
CS	BUS CHAIN (60000)	
DATA	BUS CHAIN ACKNOWLEDGE (60000)	
CL153	BUS LATCH SLOWDOWN (CHIPS)	
DL1	CHIP MEMORY ACCESS (CHIPS)	
DR	BUS REQUEST (60000)	
DVST	DEVICE BUS (PARALLEL PORT)	
CSA/ZV	COLUMN ADDRESS STROBE (ORAH)	
CCG/CLKO	COLOR CLOCK / QUADRATURE (CHIPS)	
LDMS	7.15909 MHz QUADRATURE CLOCK (CHIPS)	
CHMS	MEDIA CHANGE (LOFFPT)	
CLKR/W	READ-TIME CLOCK READ / WRITE (R/C)	
COMP	MONOCHROME CODES (V/L VIDEO LYDCK)	
CSINC	COMPOSITE SYNC (VIDEO)	
CIS	CLOCK TO SEND (AS232 PORT)	
D(15:0)	PROCESSOR DATA BUS (60000)	
DIR	STEP DIRECTION (LOFFPT)	
USRD	DISK READ DATA (LOFFPT)	
UKWD	DISK WRITE DATA (LOFFPT)	
DKWL	DISK WRITE LENGTH (LOFFPT)	
ORAL	ORAH DATA REQUEST LINE (CHIPS)	
ORAL(6:0)	ORAH ADDRESS BUS (ORAH)	
ORAL(15:0)	ORAH DATA BUS (ORAH)	
OR	ORAH SEL REPLY (AS232 PORT)	
VIDCK	DATA TRANSFER ACKNOWLEDGE (60000)	
VIR	DATA TERMINAL REPLY (AS232 PORT)	
EXTICK	EXTERNAL ENHANCED CLOCK (60000)	
F(12:0)	EXPANSION PROMPT / R/C TASK	
F(16:0)	FUNCTION CODE (60000)	
F(16:0)	FIRE BUTTON OZ (JOYSTICK)	
HLL	PROCESSOR HOLD (60000)	
HSTHC	HORIZONTAL SYNC (VIDEO)	
INDCK	INDEX PULSE (LOFFPT)	
IND(2:3,6)	INDEX/ARBITER REQUEST (CHIPS)	
INTSEL	I/O RESET	
INT(2:0)	INTERUPT PRIORITY LEVEL (60000)	
ABLOCK	KEYBOARD CLOCK (INTERNAL)	
ZVORAH	KEYBOARD DATA (KEYBOARD)	
RESET	KEYBOARD RESET (INTERNAL)	
US/MS	UPPER / LOWER DATA STROBES (60000)	
LED	POWER ON LED / AUDIO FILTER DISABLE	
LLT/RIGHT	LEFT / RIGHT AUDIO (AUDIO)	

SIGNAL	DESCRIPTION (AREA)	PAGES
LPEN	LIGHT PEN (TRIGGER / JOYSTICK)	
DIR	MOVIE ON (LOFFPT)	
DIR0	MOVIE ON - DRIVE 0 (LOFFPT)	
DIR1/DIRH	MOVIE 0 QUADRATURE V/H (JOYSTICKS)	
DIR2/DIRV	MOVIE 1 QUADRATURE V/H (JOYSTICKS)	
OVL	OVERLAY NON OVER REQ	
OVR	OVERLAY SYSTEM OCCURING	
TRVLSW	DEMOLOCK PANEL SWITCH (VIDEO)	
TRVLSW0	PAL LINES 0-271 (JOYSTICKS)	
TRVLSW1	PAL LINES 1-271 (JOYSTICKS)	
PCV	PAPER OUT (PARALLEL PORT)	
PCD(7:0)	PARALLEL PORT DATA (PARALLEL PORT)	
RDEN	RAM ENABLE (CHIPS)	
RDEN	CHIP REGISTER ENABLE (CHIPS)	
RSOZ1	RAM ADDRESS STROBE (ORAH)	
RDY	WRITE READY (LOFFPT)	
RESET	GENERAL RESET	
RS(15:0)	REGISTER ADDRESS BUS (CHIPS)	
R/OZ0	RD / DRAM / DLVC (VIDEO)	
R1	RANDOM INDICATOR (AS232 PORT)	
RDEN	RAM ENABLE (ORAH)	
RIS	REQUEST TO SEND (AS232 PORT)	
RST	PROCESSOR RESET (60000)	
RVD	RECEIVE DATA (AS232 PORT)	
RM	PROCESSOR READ/WRITE (60000)	
SEL	SELECT (PARALLEL PORT)	
SEL(3:0)	DRIVE SELECT (LOFFPT)	
SEL	DRIVE SELECT (LOFFPT)	
STEP	STEP IN/OUT COMMAND (LOFFPT)	
TRK0	TRACK ZERO SENSE (LOFFPT)	
TRK	TRACK DATA (AS232 PORT)	
VHM	VALID MEMORY ADDRESS (60000)	
VPA	VALID PARALLEL ADDRESS (60000)	
VSYNC	VERTICAL SYNC (VIDEO)	
WE	WRITE ENABLE (ORAH)	
WRD1	WRITE PROTECT SENSE (LOFFPT)	
XCLK	EXTERNAL DEMOLOCK CLOCK (VIDEO)	
XCLKEN	EXTERNAL CLOCK ENABLE (VIDEO)	
XRDY	EXTERNAL DATA READY	

.. RESULT CARD AND THE STUFF ..

KEY COMPONENTS

REF	CHIP	DESCRIPTION	PAGE
U1	68000	68000 PROCESSOR (ORAH)	2
U2	8371	ORAH (ORAH ADDRESS)	6
U3	8371	ORAH	6
U4	3203	LISA I/O DEHISL	4
U5	70022E	ORAH ARITH (ORAH ASIC)	2, 11
U6	8651	RAM (RAM 150 MS)	10
U7-8	8520	DRIVE 0/1 (1 MHz)	7
U10-11	28F10	FLASH MEMORY (PARALLEL)	10
U12	74AL14501	VIDEO ENCODER	4
U13	6570	3840X RAM (ORAH MPU)	9
U14	68555	RESET LINES	2
U15	LF347	OPAMP OR AMP	ALT
	LF004	OPAMP OR AMP	ALT
U16-17	6851	ORAH (ORAH 100 MS)	3
U18-19	6851	ORAH (ORAH OPTIONAL)	3
U20	39122	ARITHMETIC (ORAH ASIC)	2
U21	1498	LINE DRIVER	7
U22	1499	LINE RECEIVER	7
U23	01101	TRIPLE 8-BIT VIDEO OR	4
X1	05C	TTL 28.63636 MHz MISC	2
	05C	TTL 28.63636 MHz PAL	ALT
7451	7410	4-36V 19M7 PAL GUARD	4
7421	7410	36VZ LATCHED ACKNOWLEDG	9
X2	655	PAL VIDEO MODULATOR	4
	655	655C VIDEO MODULATOR	4

REV 3. PCB

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